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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/436,062	11/08/1999	CRAIG W. WARNER	10991087-1	6095
7590	04/01/2004		EXAMINER	
HEWLETT PACKARD COMPANY INTELLECTUAL PROPERTY ADMINISTRATION PO BOX 272400 FORT COLLINS, CO 805289599			FERRIS, DERRICK W	
			ART UNIT	PAPER NUMBER
			2663	(3)

DATE MAILED: 04/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/436,062	WARNER, CRAIG W.
	Examiner	Art Unit
	Derrick W. Ferris	2663

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 04 March 2004.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-17,19-22,24 and 25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-17,19-22,24 and 25 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 08 November 1999 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) All b) Some * c) None of:

1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.

5) Notice of Informal Patent Application (PTO-152)

6) Other: _____.

DETAILED ACTION

Response to Amendment

1. **Claims 1-17,19-22, and 24-25** as amended are still in consideration for this application.

Applicant has amended independent claims 1 and 16.

2. Examiner does **not withdraw** the obviousness rejection to *Galles* in view of *Stallings* for Office action filed 12/17/2003. In addressing applicant's arguments in the response filed 03/04/2004, the examiner has grouped the claims into the following two groups: group I (independent claims 1, 6, 11, and 16) and group II (dependent claims 24-25). Each of these groups will be further addressed below.

Group I (independent claims 1, 6, 11, and 16):

Applicant first claims (see applicant's remarks filed 03/04/2004 at pages 10-11) the following limitation (or equivalent) was not addressed by examiner "*wherein each subsequent intermediate node includes routing means configured to route a data packet associated with the data packet header in response to the next subsequent node's egress port independent of the state of a routing table associated with the node*". Examiner respectfully disagrees. The above-limitation was addressed in the examiner's remarks filed 12/17/2003. Please find similar remarks below in addressing applicant's concern. With respect to source logic in the source node to identify a data route from the source node to the destination node, examiner notes *Galles* teaches routing a packet based on a local routing table such that each router along the path consults a routing table (e.g., see at least column 1, lines 59-64). In addition, please see at least column 2, lines 29-38 (emphasis added) with respect to pipelining where the header already contains the egress port identifier of the current router. In other words, the route is already

predefined by the source node and is updated if necessary by each router via the local routing tables (e.g., see at least column 16, lines 25-35). Thus *Galles* teaches the limitation of source logic in the source node to identify a data route from the source node to the destination node in response to the next subsequent node's egress port independent of the state of the routing table associated with the [intermediate] node using a reasonable but broad interpretation of independent.

Second applicant argues (see applicant's remarks filed 03/04/2004 at pages 11-13) that the *Stallings* reference does not teach all three limitations found in a header. Specifically applicant argues an egress port, a current hop count, and a total number of hops in the data route are not taught by *Stallings*. It appears applicant has misconstrued the examiner's rejection. At issue are not these specific three elements, but whether it would have been obvious to place all three elements into a packet header. As pointed out by the examiner, the examiner considers all three elements taught either explicitly or inherently by *Galles*. Thus at issue is not the three elements but whether it would have been obvious to one skilled in the art prior to applicant's invention to put these three elements in a header.

Third, applicant argues motivation (see applicant's remarks filed 03/04/2004 at pages 14-20) which is closely tied to the second issue mentioned above. The examiner has clarified the motivation below. Also note that a current hop count is either expressly or inherently taught by *Galles*. The examiner also addressed the hindsight issue in addressing the motivation (see below).

Group II (dependent claims 24-25

Applicant argues fundamentals of the obviousness rejection. Examiner has cleaned up the rejection based on applicant's comments.

Claim Objections

3. **Claim 25** is objected to because of the following informalities: please add a comma between an egress indicator and a current hop count at line 4. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. **Claims 1-17 and 19-22** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No., 5,721,819 to Galles et al. ("Galles") in view of "Data and Computer Communications" to Stallings.

As to **claims 1, 6, 11 and 16**, *Galles* discloses a programmable distributed routing system and method using routing tables for a network, and more specifically towards a multi-processor environment [column 1, lines 16-24]. Using the example shown in figures 16 and 17, examiner notes *Galles* discloses a number of nodes such as a source node (e.g., an originating device 1604), an intermediate node (e.g., router 204c), and a destination node (e.g., target device 1608) [column 18, lines 1-60]. Examiner notes that *Galles* discloses, using a broad but reasonable interpretation, source logic, routing logic, and destination logic (also referred to as path identification means, routing means and

destination means) to identify, transmit, route, and detect respectively. In particular, each of the nodes has an ingress port and an egress port (note that one skilled in the art would recognize that originating device 1604 and target device 1608 have both an ingress and egress port depending on the path of the packet as shown in relation to figures 16 and 18 of *Galles*). With respect to source logic also see at least column 16, lines 25-45 of *Galles*. With respect to an egress port of a next subsequent node, a current hop count, and a total hop count see at least figures 13 and 17 of *Galles* where an egress port is shown as a vector field, and a current hop count and total hop count are easily derived from the port vectors. In other words, the hop values are either expressly or inherently taught by the *Galles* reference. In addition, since *Galles* further teaches the concept of pipelining where the vector already contains the egress port identifier of the current router, *Galles* teaches the further limitation of each subsequent intermediate node includes routing means configured to route a data packet associated with the data packet header in response to the next subsequent node's egress port independent of the state of a routing table associated with the node using a reasonable but broad interpretation of independent.

Galles is silent or deficient on whether the above-mentioned limitations of a next subsequent node, a current hop count, and a total hop count are found in a packet header. In particular, as mentioned above, *Galles* either inherently teaches or expressly teaches that these limitations are found in a vector but may be silent as to whether they are found specifically in a header of the packet/vector.

Stallings teaches that it is well known in the art to place such limitations in a packet header.

Thus the examiner purposes to modify the *Galles* reference to further clarify that the above three limitations are placed in a packet header.

Hence examiner notes that it would have been obvious to one skilled in the art prior to applicant's invention to place a next subsequent node, a current hop count, and a total hop count in a packet header. One skilled in the art would be motivated to place the vector information in the header portion since the header portion typically contains "routing information" such as address information and hop count. As further support, *Stallings* cures the above-cited deficiency by teaching that it is well known in the art to put a total hop count as well as routing information into a packet header such as an IP header (e.g., see figure 16.7 on page 544 of *Stallings* where the TTL contains the router hops). One motivation for placing this information in a header is so the router can easily locate information within a defined packet structure. Thus *Stallings* provides the support and motivation for why someone skilled in the art would place an egress port, a current hop count and total hop count in a packet header. Furthermore, *Stallings* provides further motivation by disclosing that hop counts are represented as a single field as opposed to being derived from the vector information (e.g., see the TTL field in the IP header in figure 16.7).

As to **claims 2 and 7**, examiner notes this example also shows a return route path [column 18, lines 62-67; column 19, lines 1-25]. Noted specifically is the source port

stored in the vector packet configuration. Examiner also notes a total hop count is shown (see reasoning in rejection for claim 1).

As to **claims 3 and 8**, *Galles* discloses a routing table for each router (including a source node).

As to **claims 4 and 9**, examiner notes the reasoning behind the rejection for claim 1 shows that it would have been obvious to a skilled artisan to decrement the hop count (indirectly).

As to **claims 5 and 10**, *Galles* broadly discloses replacing the destination port with the source port of the intermediate node (e.g., see figure 17). In particular, the threshold is reached when the END value is reached with respect to the port vectors (i.e., examiner notes a reasonable but broad interpretation of port vectors).

As to **claim 12**, again as mentioned in the rejection for claim 12, it would have been obvious to a skilled artisan prior to applicant's invention to include a total hops value (i.e., same motivation applies). *Galles* also broadly discloses recording at least one source port value in the data packet (for the return path).

As to **claim 13**, *Galles* discloses at least one routing path between source and destination node.

As to **claim 14**, examiner notes that it would have been obvious to a skilled artisan prior to applicant's invention to decrement the current hop count (see the reasoning behind the rejection for claim 11 in that the same motivation applies).

As to **claim 15**, see the reasoning behind the rejection for claim 13. Again, *Galles* broadly discloses an act of replacing.

As to **claim 17**, figure 17 clearly shows when a packet has arrived at the destination node (i.e., target device 1608).

As to **claim 19**, examiner notes that a header 1304 can further contain a source port value (i.e., ingress port) for the purpose of re-routing [column 18, lines 34-37].

As to **claims 20-22**, as shown in figure 17, the receipt may be acknowledged using the alterative embodiment by swapping the destination and source port values using a reasonable but broad interpretation of “swapping”. Examiner notes that the same reasoning also applies with respect to hop count as mentioned in the rejection for claim 1. Examiner also notes that the return routing is performed independently of the routing table [column 18, lines 61-67; column 19, lines 1-25].

6. **Claims 24 and 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No., 5,721,819 to Galles et al. (“*Galles*”) in view of “Data and Computer Communications” to *Stallings*, and in further view of “A Queuing Model for Wormhole Routing with Timeout” to *Hu et al.* (“*Hu*”)

As to **claim 24**, *Galles* is silent or deficient to checking for a time-out value. Examiner notes that it would have been obvious to a skilled artisan prior to applicant’s invention to use a time-out value to avoid deadlock problems in a multiprocessor network.

Hu discloses using a time-out to avoid deadlock [page 585]. Thus examiner purposes to modify *Galles* to further include a time-out value wherein acknowledging receipt further comprises a timeout value.

Thus examiner notes that it would have been obvious to one skilled in the art prior to applicant's invention to further include a time-out value wherein acknowledging receipt further comprises a timeout value. One skilled in the art would be motivated to perform the proposed modification for the purpose of avoiding deadlocking. In particular, *Galles* discloses performing deadlock free routing [column 2, lines 4-5] such that routing tables can be reprogrammed to account for changes in the network configuration such as deadlock and *Hu* discloses using a time-out to avoid deadlock [page 585]. Thus the references in combination further teach the concept of using a time-out to avoid deadlocking.

As to **claim 25**, as mentioned above *Hu* discloses deadlocking and the use of a timeout value to avoid deadlock. In particular, *Hu* discloses that a packet should be rebuffered if deadlock occurs. *Galles* further clarifies what happens during the rebuffering process at column 2, lines 1-11. In particular, tables can be reprogrammed such that vector paths are updated.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Derrick W. Ferris whose telephone number is (703) 305-4225. The examiner can normally be reached on M-F 9 A.M. - 4:30 P.M. E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on (703) 308-5340. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Derrick W. Ferris
Examiner
Art Unit 2663

DWF


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